WHAT IS CLAIMED IS:

1. A power interface circuit for coupling an adapter output voltage from an adapter unit to a system power input of a system comprising:

switch circuitry for coupling said adapter output voltage to a said system power input in response to a first logic state of a first control signal;

a reference circuit for generating first and second reference voltages and a start timer signal in response to a polarity signal generated from said adapter output voltage;

a first timer circuit generating a first timer signal in response to a first logic state of said start timer signal, wherein said first timer output has a first logic state for a first time interval and a second logic state after said first time interval ends;

a second timer circuit generating a second timer signal in response to said first logic state of said start timer signal, wherein said second timer output has a first logic state for a second time interval and a second logic state after said second time interval ends;

circuitry for generating a power correct signal in response to said first and second reference voltages, a sense voltage corresponding to said adapter output voltage, and said first timer signal, said power correct signal having a first logic state if said adapter output voltage is within a voltage range set by said first and second reference voltages and said second timer signal has said second logic state; and

logic circuitry receiving said power correct signal, said first timer signal, said second timer signal, and generating said first control signal and an out of range signal, wherein said first control signal has said first logic state if said out of range signal has a first logic state and said second timer signal has said second logic state.

2. The power interface circuit of claim 1, wherein said logic circuit further comprises a low voltage level circuit receiving said system power input and generating a low level signal, said low level signal having a first logic state if a

system voltage of said system power input is below a predetermined low voltage level.

3. The power interface circuit of claim 2, wherein said logic circuit further comprises a shut down latch enabled by said first logic state of said start timer signal and generating said out of range signal, wherein said out of range signal has a first logic state if said power correct signal has said second logic state and said first timer signal has said second logic state or said second timer signal has said second logic state and said low level signal has said first logic state.

4. The power interface circuit of claim 1, wherein said switch circuitry comprises:

a first electronic switch for coupling said adapter output voltage to a sense node in response to a first logic state of a gate control signal;

a diode having an anode coupled to said adapter output voltage and a cathode coupled to said sense node;

a second electronic switch for coupling said sense node to said system power input in response to said first logic state of said gate control signal; and

a gate control circuit for generating said gate control signal in response to said first control signal.

5. The power interface circuit of claim 4, wherein said logic circuitry further comprises charge circuitry for coupling said sense node to said system power input in response to a first logic state of a third control signal, wherein said third control signal has said first logic state if said power signal has said first logic state and said second time output signal has said first logic state.

6. The power interface circuit of claim 4, wherein said gate control circuit comprises a third electronic switch that is gated ON generating said first logic state of said gate control signal when said first control signal has said first logic state.

7. The power interface circuit of claim 1, where said sense voltage is generated by a sense circuit comprising:

a first resistor having a first terminal coupled to said adapter output voltage and a second terminal; and

a second resistor having a first terminal coupled to said second terminal of said first resistor and a second terminal coupled to a ground potential, wherein said sense voltage is generated at said second terminal of said first resistor.

8. The power interface circuit of claim 5, wherein said charge circuitry comprises:

a first resistor having a first terminal coupled to said sense node and a second terminal;

a P type field effect transistor (PFET) having a source terminal coupled to said second terminal, a drain terminal coupled to said system power input and a gate terminal;

a second resistor having a first terminal coupled to said gate terminal of said PFET and a second terminal; and

a N type FET (NFET) having a drain terminal coupled to said second terminal of said second resistor, a source terminal coupled to a ground potential and a gate terminal coupled to said third control signal.

9. The power interface circuit of claim 4 further comprising a fourth electronic switch for coupling a battery supply unit to said system power input in response to said first logic state of said first control signal.

10. The interface circuit of claim 9, wherein said fourth electronic switch comprises:

a resistor having a first terminal coupled to said first control signal and a second terminal coupled to a ground potential; and

a PFET having a drain terminal coupled to an output of said battery unit, a source terminal coupled to said system power input, and a gate terminal coupled to said first terminal of said resistor, wherein an anode of a body diode of said PFET is coupled to said drain terminal and a cathode of said body diode is coupled to said source terminal.

11. The power interface circuit of claim 1, wherein said sense voltage is coupled to a cathode of a diode and an anode of said diode is coupled to a ground potential.

12. The power interface circuit of claim 1 further comprising a reverse voltage circuit coupled to said adapter output voltage for indicating said preferred polarity of said adapter output voltage.

13. The power interface circuit of claim 12, wherein said reverse voltage circuit comprises:

a resistor having a first terminal coupled to said adapter output voltage and a second terminal; and

a light emitting diode having an anode coupled to a first node and a cathode coupled to said second terminal of said resistor, said first light emitting diode indicating a reverse voltage condition when ON.

14. The power interface circuit of claim 1, wherein said out-of-range voltage is coupled to an anode of a light emitting diode having a cathode coupled to a ground potential, said light emitting diode indicating an out-of-range voltage condition when ON.

15. The power interface circuit of claim 13, wherein said first node is coupled to a ground potential.

16. The power interface circuit of claim 13, wherein said first node is coupled to a polarity circuit for generating a reverse voltage alert signal.

17. The power interface circuit of claim 16, wherein said polarity circuit comprises:

a NPN transistor having an emitter terminal coupled to said first node, a base terminal coupled to a ground potential and a collector terminal;

a sense resistor having a first terminal coupled to a power supply voltage and a second terminal coupled to said collector terminal; and

an inverter logic gate powered by said power supply voltage and having an input coupled to said second terminal and an output generating said reverse voltage alert signal.

18. The power interface circuit of claim 17, wherein said reverse voltage alert signal is coupled to said system for notifying a user of said system of a reverse voltage condition.

19. A battery operated system comprising:

a central electronics unit coupled to a system power input for powering said system;

an adapter input for receiving an adapter output voltage from an alternating current (AC) adapter unit;

a power interface circuit for coupling an adapter output voltage of said AC adapter unit to said system power input, wherein said power interface circuit further comprises;

switch circuitry for coupling said adapter output voltage to a said system power input in response to a first logic state of a first control signal;

a reference circuit for generating first and second reference voltages and a start timer signal in response to a polarity signal generated from said adapter output voltage;

a first timer circuit generating a first timer signal in response to a first logic state of said start timer signal, wherein said first timer output has a first logic state for a first time interval and a second logic state after said first time interval ends;

a second timer circuit generating a second timer signal in response to said first logic state of said start timer signal, wherein said second timer output has a first logic state for a second time interval and a second logic state after said second time interval ends;

circuitry for generating a power correct signal in response to said first and second reference voltages, a sense voltage corresponding to said adapter output voltage, and said first timer signal, said power correct signal having a first logic state if said adapter output voltage is within a voltage range set by said first and second reference voltages and said second timer signal has said second logic state; and

logic circuitry receiving said power correct signal, said first timer signal, said second timer signal, and generating said first control signal and an out of range signal,

wherein said first control signal has said first logic state if said out of range signal has a first logic state and said second timer signal has said second logic state.

20. The system of claim 19, wherein said logic circuit further comprises a low voltage level circuit receiving said system power input and generating a low level signal, said low level signal having a first logic state if a system voltage of said system power input is below a predetermined low voltage level.

21. The system of claim 20, wherein said logic circuit further comprises a shut down latch enabled by said first logic state of said start timer signal and generating said out of range signal, wherein said out of range signal has a first logic state if said power correct signal has said second logic state and said first timer signal has said second logic state or said second timer signal has said second logic state and said low level signal has said first logic state.

22. The system of claim 19, wherein said switch circuitry comprises:

a first electronic switch for coupling said adapter output voltage to a sense node in response to a first logic state of a gate control signal;

a diode having an anode coupled to said adapter output voltage and a cathode coupled to said sense node;

a second electronic switch for coupling said sense node to said system power input in response to said first logic state of said gate control signal; and

a gate control circuit for generating said gate control signal in response to said first control signal.

23. The system of claim 22, wherein said logic circuitry further comprises charge circuitry for coupling said sense node to said system power input in response to a first logic state of a third control signal, wherein said third control signal has said first logic state if said power signal has said first logic state and said second time output signal has said first logic state.

24. The system of claim 22, wherein said gate control circuit comprises a third electronic switch that is gated ON generating said first logic state of said gate control signal when said first control signal has said first logic state.

25. The system of claim 19, where said sense voltage is generated by a sense circuit comprising:

a first resistor having a first terminal coupled to said adapter output voltage and a second terminal; and

a second resistor having a first terminal coupled to said second terminal of said first resistor and a second terminal coupled to a ground potential, wherein said sense voltage is generated at said second terminal of said first resistor.

26. The system of claim 23, wherein said charge circuitry comprises:

a first resistor having a first terminal coupled to said sense node and a second terminal;

a P type field effect transistor (PFET) having a source terminal coupled to said second terminal, a drain terminal coupled to said system power input and a gate terminal;

a second resistor having a first terminal coupled to said gate terminal of said PFET and a second terminal; and

a N type FET (NFET) having a drain terminal coupled to said second terminal of said second resistor, a source terminal coupled to a ground potential and a gate terminal coupled to said third control signal.

27. The system of claim 22 further comprising a fourth electronic switch for coupling a battery supply unit to said system power input in response to said first logic state of said first control signal.

28. The system of claim 27, wherein said fourth electronic switch comprises:

a resistor having a first terminal coupled to said first control signal and a second terminal coupled to a ground potential; and

a PFET having a drain terminal coupled to an output of said battery unit, a source terminal coupled to said system power input, and a gate terminal coupled to said first terminal of said resistor, wherein an anode of a body diode of said PFET is coupled to said drain terminal and a cathode of said body diode is coupled to said source terminal.

29. The system of claim 19, wherein said sense voltage is coupled to a cathode of a diode and an anode of said diode is coupled to a ground potential.

30. The system of claim 19 further comprising a reverse voltage circuit coupled to said adapter output voltage for indicating said preferred polarity of said adapter output voltage.

31. The system of claim 30, wherein said reverse voltage circuit comprises:

a resistor having a first terminal coupled to said adapter output voltage and a second terminal; and

a light emitting diode having an anode coupled to a first node and a cathode coupled to said second terminal of said resistor, said first light emitting diode indicating a reverse voltage condition when ON.

32. The system of claim 19, wherein said out-of-range voltage is coupled to an anode of a light emitting diode having a cathode coupled to a ground potential, said light emitting diode indicating an out-of-range voltage condition when ON.

33. The system of claim 31, wherein said first node is coupled to a ground potential.

34. The system of claim 31, wherein said first node is coupled to a polarity circuit for generating a reverse voltage alert signal.

35. The system of claim 34, wherein said polarity circuit comprises:

a NPN transistor having an emitter terminal coupled to said first node, a base terminal coupled to a ground potential and a collector terminal;

a sense resistor having a first terminal coupled to a power supply voltage and a second terminal coupled to said collector terminal; and

an inverter logic gate powered by said power supply voltage and having an input coupled to said second terminal and an output generating said reverse voltage alert signal.

36. The system of claim 35, wherein said reverse voltage alert signal is coupled to said system for notifying a user of said system of a reverse voltage condition.